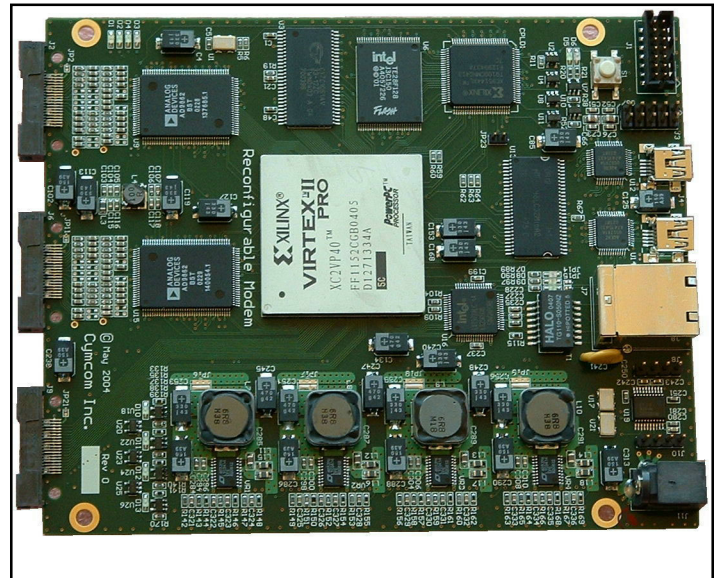


### BOARD FEATURES

- Xilinx Virtex-II Pro FPGAS (V2P20 – V2P50)
- 16 Mbytes FLASH
- 2 Mbytes SRAM
- 64 Mbytes SDRAM
- Two AD9862 Mixed-Signal Front-End Processors
  - four 12-bit 64 MSPS Sampling A/D converters
  - four 14-bit 128 MSPS D/A converters
  - six general purpose D/A converters
  - four general purpose A/D converters
- Digital I/O Connector (34-bits)
- (2) Mixed Analog/Digital Connector
- 10/100 BaseT Ethernet PHY (MII) & RJ-45 connector
- Two USB 2.0 Ports
- Two RS-232 Ports
- JTAG Interface
- Reconfigurable from SRAM using Ethernet or USB providing hot reconfigurability.
- Four externally synchronized switching regulators optimized for low switching noise (3.3V, 3.0V, 2.5V, 1.5V)
- On-board Oscillators at 100, 60, 44 MHz
- Eight digital test pins and four programmable LEDs

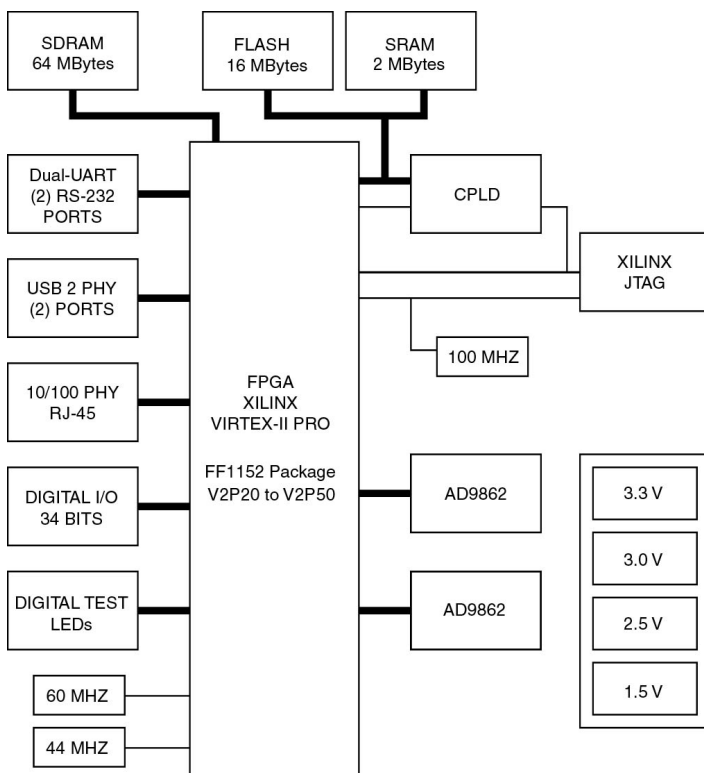
### DXV2P-D1 DEVELOPMENT BOARD



### APPLICATIONS

- Broadband Wireless Systems
  - Wi-Fi, Bluetooth, Cellular
- Broadband Wireline Systems
  - Cable and DSL Modem Development
- Digital Communications
- Standard and Proprietary Data Links
- Digital Signal Processing
- Software Radio Development
- Surveillance, covert communications, Direction Finders
- Specialized Radar, sonar, or ultra-sound development

### DXV2P-D1 FUNCTIONAL BLOCK DIAGRAM



### GENERAL DESCRIPTION

The DXV2P-D1 is a low-cost flexible development platform designed for use as a tool in the implementation of a wide range of communications, networking, and signal processing systems. This single board solution provides high-performance A/D and D/A converters with digital mixing and digital filtering, two immersed PowerPC processors and all the flexibility of a high-performance FPGA fabric. Combine all this with several standard communications interfaces and you have a complete system that can be “hot” reconfigured from SRAM over Ethernet, USB, or RS-232 making this the ideal development platform for your communications or processing applications. The mixed signal analog/digital ports have 16-bits of digital I/O, one Global Clock and the analog signals. The digital port has 34-bits of digital I/O.

The Xilinx Virtex-II Pro delivers superior capabilities for high performance and high-density designs with IP, PCI, Viterbi, Reed-Solomon, Rapid I/O and other core modules making the Virtex-II Pro family ideal for telecommunications, wireless, networking, video and DSP applications. The Virtex-II Pro incorporates two immersed PowerPC processors, 20K to 50K Logic Cells, 1 Mbit to 4 Mbits of multi-ported Block RAM, dedicated 18x18 bit Multipliers, and the full flexibility of the highest performance FPGA fabric available. These devices also incorporate multiple digital clock management blocks with on-chip digital controlled impedance terminations providing flexible clocking. This board uses the FF1152 package and can accept the XC2VP20 through the XC2VP50.

The Analog Devices AD9862 Mixed-Signal Front-End (MxFE) processor is optimized for high-performance broadband communications and signal processing applications. The transmission section has six stages: dual 14-bit 128 MSPS DACs with programmable gain amplifiers, coarse quadrature modulation mixer, interpolations stage, fine quadrature modulation mixer, Hilbert filter and data input circuitry. The receive section has five stages: input buffers, programmable gain amplifiers, dual 12-bit 64 MSPS ADC, decimation filter, and Hilbert filter. Combine all of the features of the MxFE processor and the Virtex-II Pro and this platform has the components needed to develop a wide range of communications and signal processing applications. Add to this, an RF sub-systems that connects to the V2P mixed signal port and you have a complete development system.

The DXV2P-D1 also has a 10/100 mbit Ethernet physical layer, two USB 2 ports, two RS-232 ports, six Auxiliary DACs, four Auxiliary ADCs, and a general purpose digital I/O port attached to the Virtex-II Pro device. These general-purpose I/O interfaces provide a variety of ways to transfer data and control telemetry between the DXV2P-D1 and other processors or computers. DSP Systems has a growing list of interface modules for the analog and digital I/O ports on the VP2. Additionally, complete documentation is available to enable users to design interface modules to meet their specific needs. The digital port is also compatible with an Agilent logic analyzer.

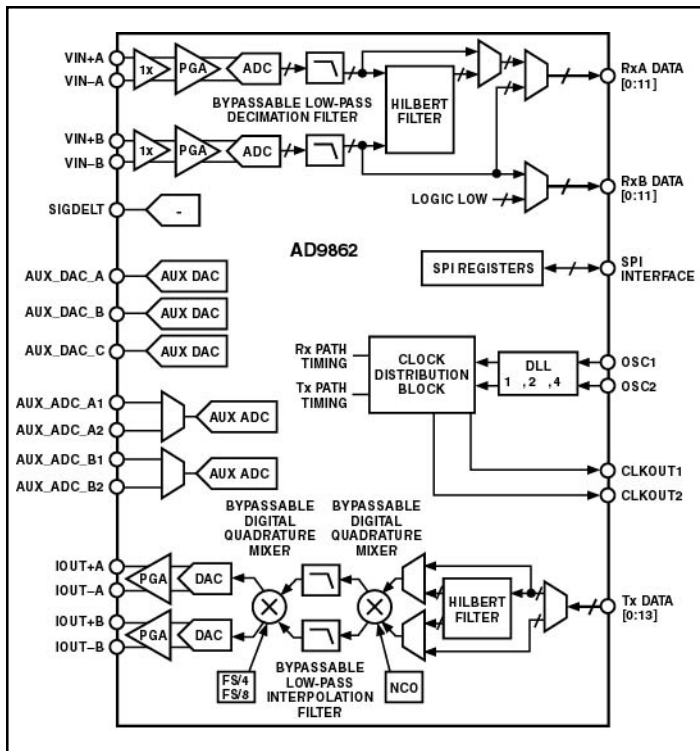
The on-board regulators are optimized for use with the analog systems and require only 5V input.



## XILINX VIRTEX-II PRO FEATURES

- Superior Programmable Logic Architecture
  - Built on a 130 nm, 9-layer copper process technology
  - 20K to 50K logic cells
  - 400+ MHz clock rates
  - Higher performance and lower power consumption than earlier generation technologies
  - Unmatched optimization enables stuffing more logic per area driving down unit costs
- Highest Scalability and Widest Choice
  - 4 devices available in this package
  - Move up or down in features, density, I/O, and performance
- Advanced System Features
  - Embedded and distributed memory
  - Digital Clock Management for on-chip/off-chip clock synthesis and synchronization
  - XCITE digitally-controlled I/O impedance improves signal integrity and reduces board space
  - Full/partial FPGA reconfiguration gives your products field upgradability
  - TeraMAC/s DSP Performance
  - Up to 232 18X18 embedded multipliers
  - Extensive library of DSP algorithms
  - DSP tools such as The MathWorks MATLAB™/ Simulink™, the Xilinx System Generator for DSP, and Cadence SPW
- Advanced Processing
  - Up to two 400MHz, 600+ DMIPS embedded IBM PowerPC 405 Processor hard cores
  - Industry's fastest soft processing solution with MicroBlaze™ core
- Fastest Development Tools
  - Easiest tools for programmable logic and embedded software
  - 6x faster compile times than closest alternative
  - Over 200 IP cores from Xilinx and partners
  - Real time debug using ChipScope™ Pro tools

## AD9862 FUNCTIONAL BLOCK DIAGRAM



## ORDERING INFORMATION

- DXV2P-D1-20-x with XC2VP20-x
- DXV2P-D1-30-x with XC2VP30-x
- DXV2P-D1-40-x with XC2VP40-x
- DXV2P-D1-50-x with XC2VP50-x

(x) is speed grade of FPGA. Currently -5, -6, -7

## AD9862 FEATURES

- Dual Converter Receive and Dual Converter Transmit Signal Paths
- Receive Signal Path Includes
  - Two 12-bit, 64 MSPS Sampling A/D converters
  - Input buffers
  - Digitally programmable gain amplifiers
  - Low-pass decimation filter and digital Hilbert filter
  - Integrated or external references
- Transmit Signal Path Includes
  - Two 14-bit, 128 MSPS D/A converters
  - Digitally programmable output current
  - Independent programmable Fine Gain and Offset control
  - Digital Hilbert and interpolations filters
  - Digitally tunable Real or Complex up-converters
- System Clocking
  - Programmable output clocks
  - Single clock operations
- Auxiliary Features
  - Three auxiliary DAC outputs
  - Two auxiliary ADC inputs
  - Sigma-Delta output